REMARKS

The application has been amended to place the application in condition for allowance at the time of the next Official Action.

Claims 1-8 and 24-30 were previously pending in the application. Claims 2 and 25 are cancelled, leaving claims 1, 3-8, 24 and 26-30 for consideration.

Claim 30 is amended to remove the word "pattern" from line 6 so that line 6 recites "at least one first metal wiring layer". Amending claim 30 in this manner is believed to address the claim objection noted in the Official Action. Amending claim 30 as above is also believed to address the 35 USC §112, second paragraph rejection noted in the Official Action.

Claims 1-8 and 24-30 were rejected as unpatentable over SHEU et al. 6,694,208 in view of applicants' disclosed prior art. That rejection is respectfully traversed.

Claim 1 is amended to include the subject matter of claim 2 and recites that a yield-rate of acceptable semi-finished semiconductor devices is found in a provisional yield-rate test. It is determined that the wafer has passed the provisional yield-rate test when the yield-rate exceeds a predetermined permissible rate.

The position set forth in the Official Action is that the SHEU reference teaches what is recited in claim 2.

However, the reference does not teach that for which it is offered.

SHEU teaches to distinguish between the types of failures. For example, main failure, single-bit failure, twin-bit failure and one-mega defect failure. As set forth on column 3, lines 17-34 of SHEU, each of the types of failures is calculated and ranked according to the magnitude of the yield loss contribution. The failure mode with the largest yield loss contribution has the greatest affect on yield loss. SHEU adjusts his equipment or processing related to the failure mode with the largest yield loss to improve his yield loss.

SHEU does not teach a predetermined permissible rate that if exceeded, then further processing continues. Rather, as set forth above, SHEU determines which failure mode has the greatest affect on yield loss and adjusts processing based on that particular failure mode, not based on whether a yield test exceeds a predetermined permissible rate.

Applicants' disclosed prior art does not overcome the shortcomings of SHEU.

The above-noted feature is missing from each of the references, is absent from the combination, and thus would not have been obvious to one having ordinary skill in the art.

Claims 3-8 depend from claim 1 and further define the invention and are also believed patentable over the cited prior art.

In addition, claim 4 recites that the basic wiring-arrangement section has a plurality of electrode pads formed on an uppermost surface thereof for carrying out a provisional yield-rate test.

Electrode pad 58' of applicants' disclosed prior art is offered for this teaching.

However, applicants' disclosed prior art does not perform a provisional yield-rate test and thus would not need a plurality of electrode pads formed on a basic wiring section to carry out the provisional yield-rate test.

Moreover, page 35, line 29 through page 36, line 4 of the application as filed, disclose that electrode pads 58' and a plurality of conductive leads 60' are simultaneously formed on the insulation layer 54' at an outer peripheral area surrounding the uppermost metal circuit pattern layer 56'. Such insulation layer 54' is formed on top of and after the basic wiring-arrangement section has been formed. Applicants' disclosed prior art does not teach or suggest a plurality of electrode pads formed on an uppermost surface of a basic wiring-arrangement section (first metal wiring layer).

SHEU does not teach or suggest what is recited in claim 4. Accordingly, claim 4 is believed patentable regardless of the patentability of the claims from which it depends.

Independent claim 24 is amended to include the subject matter of claim 25 and recites that the first metal wiring layer

has a plurality of electrode pads formed on an uppermost surface thereof for carrying out a provisional yield-rate test.

SHEU teaches a method of differentiating between failure modes to adjust yield rate. SHEU does not provide any specifics as to the structure of the chips formed in SHEU. Therefore, SHEU could not teach a first metal wiring layer having a plurality of electrode pads formed on an uppermost surface thereof for carrying out a provisional yield-rate test.

As set forth above with respect to claim 4, applicants' disclosed prior art does not teach or suggest this feature.

The above-noted feature is missing from each of the references, is absent from the combination, and thus would not have been obvious to one having ordinary skill in the art.

Claims 26-28 depend from claim 24 and further define the invention and are also believed patentable over the cited prior art.

Independent claim 29 recites a first metal wiring layer having a first test section and a second metal wiring layer having a second test section different than the first test section. The second test section is electrically connected to said active region (the same active region to which the first test section is electrically connected).

The position set forth in the Official Action is that SHEU inherently teaches first and second test sections electrically connected to an active region.

However, the question is not whether first and second test sections are electrically connected to an active region. Rather, the question is whether the first and second test sections are connected to said active region (the same active region).

Even if SHEU inherently teaches first and second test sections electrically connected to an active region, which applicants assert it does not, nevertheless, SHEU does not teach or suggest that the first and second test sections are electrically connected to said active region (the same active region) as recited.

It is well settled that to establish a *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. Since all the claim limitations are not taught or suggested by the prior art, *prima facia* obviousness has not been established. Reconsideration and withdrawal of the rejection as to claim 29 are respectfully requested.

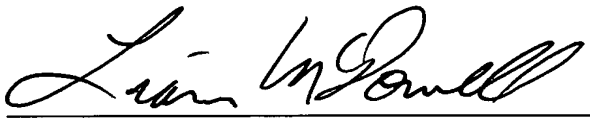
Independent claim 30 has been amended to include the subject matter of claim 2 and recites that the yield-rate of acceptable semi-finished semiconductor devices is found in the provisional yield-rate test. It is determined that the wafer has passed the provisional yield-rate test when the yield-rate exceeds a predetermined permissible rate. The analysis above regarding claim 1 is equally applicable to claim 30.

In view of the present amendment and the foregoing remarks, it is believed that the present application has been placed in condition for allowance. Reconsideration and allowance are respectfully requested.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

YOUNG & THOMPSON



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